REMARKS

Claims 1-33 are pending in the present application. Claims 1, 14, 26, 28, 30, and 32, and the specification have been amended to correct typographic errors, to respond to the rejections, and/or to further clarify the subject matter recited therein. No new matter is added by the amendments, which are supported throughout the specification and figures. In particular, the amendments are supported at least in the specification in the paragraph beginning at page 16, line 23, and inherently, as discussed below. In view of the amendments and the following remarks, favorable reconsideration of this case is respectfully requested.

The specification is objected to as not providing antecedent basis for the claimed subject matter. Specifically, the Examiner asserts that there is no support for the feature of a cache operating as a controller. However, the specification states that "[e]ach cache 20 typically comprises random access memory (RAM), such as dynamic RAM and/or solid state disks, and may also additionally comprise software" (specification; page 16, line 33, to page 17, line 1; underlining indicating amendments to the specification). Applicants submit that ***the disclosure of the caches as including software inherently discloses the caches including a processor***. As the MPEP states in regard to Inherent Function, Theory, or Advantage:

> By disclosing in a patent application a device that inherently performs a function or has a property, operates according to a theory or has an advantage, a patent application necessarily discloses that function, theory or advantage, even though it says nothing explicit concerning it. ***The application may later be amended to recite the function, theory or advantage without introducing prohibited new matter.*** In re Reynolds, 443 F.2d 384, 170 USPQ 94 (CCPA 1971); In re Smythe, 480 F. 2d 1376, 178 USPQ 279 (CCPA 1973). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of

> circumstances is not sufficient.'" In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted).

(MPEP 2163.07(a); emphasis added). Furthermore, the Examiner recognized in the Office Action dated July 2, 2007 that "software is a computer program; or instructions that make hardware work" (citing Microsoft Computer Dictionary, 5th ed.). The explicit disclosure that the caches may comprise software provides inherent disclosure that the caches include controllers. This inherent disclosure provides a basis for amending the specification to recite this function without introducing prohibited new matter, as required by the MPEP.

With the amendment of the specification to explicitly include the inherent disclosure of the caches including controllers, and the amendment of the claims to add the feature that the first, second, and third caches being implemented in three separate physical units***, comprise software, and are adapted to function as controllers*** substantially independently of each other, Applicants submit that the disclosure provides antecedent basis for the claimed subject matter. Therefore it is respectfully requested that the objections be withdrawn.

Claims 1-33 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Based on the amendments to the claims discussed above, Applicants submit that the issues with the claims are resolved, and respectfully request that the rejection be withdrawn.

Additionally, as argued previously, many of the sections of the specification used to describe the claimed cache make it apparent that references in the current disclosure to cache refer to a memory and controller combination. In particular, the each cache is described at one point as including a track location table 21 specific to the cache which gives its respective cache exact location details, on disks 12, for tracks of the range assigned to the cache (Specification;

page 18, lines 17-22). Furthermore, the specification states that "[t]rack location table 21 may be implemented as software, hardware, or a combination of software and hardware" (Specification; page 18, lines 22-24). Furthermore, the specification indicates, with respect to figure 5, that:

> In a cache response 106, each cache 20 receiving a track request from the RRI responds to the request. The response is a function of, *inter alia*, the type of request, i.e., whether the track request is a read or a write command and whether the request is a "hit" or a "miss." Thus, data may be written to the LA of the track request from the cache and/or read from the LA to the cache. Data may also be written to the RRI from the cache and/or read from the RRI to the cache. If system 10 comprises an all-to-all configuration, and the response includes writing to or reading from the LA, the cache uses its track location table 21 to determine the location on the corresponding disk of the track for the LA.

(Specification; page 28, lines 12-25). As is apparent from the quoted passage, the caches discussed in the specification include associated controllers for the purpose of reading and writing the data to the respective cache. Therefore, it is respectfully submitted that the claims as presented comply with the written description requirement.

Claims 1-8, 12-21, and 25 are rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent Publication No. 2004/0153727 to Hicken et al. (hereinafter referred to as Hicken). Applicants respectfully traverse.

Claim 1 relates to a method for managing a data storage system that includes, *inter alia*, configuring a first cache to perform at least one of the operations of retrieving data from and storing data at a first range of logical addresses (LAs) in a storage device, and configuring a second cache to perform at least one of the operations of retrieving data from and storing data at a first part of the first range of LAs. The method of amended claim 1 also includes configuring one or more third caches to perform at least one of the operations of retrieving data from and storing data at a second range of LAs in the storage device, ***the first, second and third caches***

being implemented in three separate physical units, comprising software, and adapted to function as controllers substantially independently of each other. The method of claim 1 includes detecting an inability of the second cache to retrieve data from or store data at the first part of the first range of LAs. The method of amended claim 1 further includes ***reconfiguring at least one of the one or more third caches to perform at least one of the operations of retrieving data from and storing data at the first part of the first range of LAs in response to the inability while continuing to perform at least one of the operations of retrieving data from and storing data at the second range of LAs***.

Initially, regarding the Office Action's assertion that the language "adapted to" in the above instance does not further limit the claim, Applicants respectfully disagree. As is apparent in the section of the MPEP cited by the Examiner, the phrase "adapted to" merely raises the question of a limiting effect. Applicants submit that the answer to that question in this instance is that the phrase "adapted to function as controllers substantially independently of each other" is a limitation on the recited caches in the method, and therefore is deserving of patentable weight. In fact, the limitation of a cache functioning as a controller distinguishes the instant claims from the cited prior art, and therefore the limiting effect of the language following the words "adapted to" is concrete and substantial. Applicants submit that the caches relied on in the Office Action do not operate as controllers, and are not substantially independent. In fact, the caches in Hicken rely on the CPUs shown in figure 3 to function, and each CPU apparently is adapted to operate with all of the secondary caches as well as its own primary cache. Applicants resubmit the previously presented argument regarding the allowability of the claims based on the novel feature of the caches operating as controllers substantially independently. Therefore, for at least this and the following reasons, the claims are allowable.

The Examiner relies on Hicken at paragraph 0041 as alleged disclosure of the feature of a first cache (element 339), a second cache (element 333), and a third cache (element 338) (Office Action; page 4). With respect to the feature of the first, second and third caches being implemented in three separate physical units and adapted to function as controllers substantially independently of each other, the Examiner relies on the statement in Hicken that "[c]onversely, the storage controller 370-2 maintains cache information related to management of LA2 in its primary cache memory 338 and in the secondary cache memory 334 of the storage controller 370-1" (Hicken; paragraph 0041, lines 14-17). However, the Examiner has not relied on element 334 as disclosing any of the caches recited in the claims. Furthermore, elements 339 and 338 of Hicken, which the Examiner asserts discloses the first and third caches, respectively, are controlled by the same controller, namely CPU 336 (Hicken, figure 3). Furthermore, each CPU in each controller in Hicken is capable of controlling caches in other controllers. As stated in Hicken:

> [0040] Although the storage controllers 370-1, 370-2, 370-3, 370-4 of the storage subsystem 300 of FIG. 3 are illustrated as being connected in series by the shared busses 360 for clarity of FIG. 3, the inventors disclose that each CPU 331, 336, 371, or 381 within ***each storage controller 370-1, 370-2, 370-3, or 370-4 can manipulate the secondary cache memories 334, 339, 374, or 384 of the other storage controllers via shared busses 360***. That is, the primary cache memory of every storage controller in the array of storage controllers 330 is connected to each and every secondary cache memory of every storage controller in the array of storage controllers 330 via shared bus 360.

(Hicken; paragraph 0040; emphasis added). Therefore, the various controllers in Hicken are actually sets of functional units that can be arranged in various ways and have no particular significance in the way they are arranged. In stark contrast, in the instant application, the CPU in each of the caches can only work on the cache itself. Therefore, Hicken does not disclose or

suggest the first, second and third caches being implemented in three separate physical units and adapted to function as controllers substantially independently of each other.

Additionally, Hicken does not disclose or suggest the feature of the amended claims that the caches comprise software. Therefore, for at least this additional reason, the claims are allowable.

Furthermore, the Office Action asserts that element 338 discloses the one or more third cache as claimed. However, there is no disclosure relating to reconfiguring element 338 to perform the operations of retrieving data from and storing data at logical addresses which were previously serviced by element 333, which the Office Action asserts discloses the second cache. Nor is there any disclosure that element 338 in Hicken accepts these additional functions while continuing to perform at least one of the operations of retrieving data from and storing data at the second range of LAs, as claimed. Hicken merely discloses using a backup secondary cache memory for loading data in storage when a primary cache memory fails. Therefore, for at least all of the above reasons, claim 1 is allowable.

Independent claim 14 includes a feature similar to the feature discussed above in regard to claim 1, and therefore claim 14 is allowable for at least the same reasons as claim 1 is allowable.

Claims 2-8, 12, 13, 15-21, and 25 depend from one of claims 1 and 14, and therefore each of these claims is allowable for at least the same reasons as claims 1 and 14 are allowable.

Claims 26-33 are rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent No. 6,898,666 to Henry et al. (hereinafter referred to as Henry). Applicants respectfully traverse.

Independent claims 26, 28, 30, and 32 have been amended to include a feature similar to the feature discussed above in regard to claim 1. Henry fails to disclose or suggest the feature of a plurality of interim fast-access-time caches, configured to operate ***as controllers substantially*** independently of one another, as recited in claim 26. The Office Action cites Henry at col. 5, lines 45-55, which states in its entirety:

> FIG. 5 illustrates a table which assigns certain logical block addresses to certain cache pools. When an I/O is received, the LBA is determined to be in a certain range and that range determines which cache pool is used. No matter what the logical block size is, the assignment is performed in the same manner as it is based on the LBA number. When an I/O spans multiple LBA ranges, two XOR operations are required. The assignment shown in FIG. 5 is made on a rotational basis. Accessing different LBA ranges uses separate memory complexes which use separate paths resulting in load balancing on those paths.

(emphasis added). The Examiner apparently relies on the section which indicates that different LBA ranges use separate memory complexes which use separate paths. Applicants again assert that this does not disclose the cited feature of a plurality of interim fast-access-time caches in which each of the plurality of interim fast-access-time caches ***comprise software*** and are ***configured to operate as controllers substantially independently*** of one another.

The Examiner is also reminded that it is the duty of the Examiner to specifically point out each and every limitation of a claim being rejected as per §1.104(c)(2) of Title 37 of the Code of Federal Regulations and section 707 of the M.P.E.P., which explicitly states that "the particular part relied on must be designated" and "the pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified". As previously stated, there is no indication in Henry that the cache pools discussed therein are ***configured to operate as controllers substantially independently*** of one another, and therefore, claim 26 is allowable over Henry.

Independent claims 28, 30, and 32 include features similar to the feature discussed above in regard to claim 26, and therefore each of these claims is allowable for at least the same reasons as claim 26 is allowable.

Claims 27, 29, 31, and 33 depend from one of claims 26, 28, 30, and 32, and therefore each of these claims is allowable for at least the same reasons as claims 26, 28, 30, and 32 are allowable.

Claims 9-11 and 22-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hicken in view of D. Karger et al. "Consistent Hashing and Random Trees: Distributed Caching Protocols for Relieving Hot Spots on the World Wide Web," Proceedings of the 29th ACM Symposium on Theory of Computing, pages 654-663, May 1997 (hereinafter referred to as Karger). Applicants respectfully traverse.

The addition of Karger fails to cure the critical deficiency discussed above in regard to Hicken as applied against claims 1 and 14. Therefore, since each of claims 9-11 and 22-24 depend from one of claims 1 and 14, each of these claims is allowable for at least the same reasons as claims 1 and 14 are allowable.

CONCLUSION

In view of the remarks set forth above, this application is believed to be in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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